II. LISTING OF THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1-4. (Canceled).

5. (Currently Amended) A method of forming a semiconductor device structure, the method comprising the steps of:

bonding a first wafer having a first surface direction atop a second wafer having a different second surface direction; the first wafer including a buried oxide layer;

forming an opening through the first wafer to the second wafer; ~~and~~

forming a region in the opening coplanar with a surface of the first wafer, wherein the region has the second surface direction;

implanting an oxygen; and

annealing to re-form the buried oxide layer in the region that was removed when the opening was formed.

6. (Canceled).

7. (Currently Amended) The method of claim [[6]] 5, further comprising the step of forming a first type gate electrode on the region, and a second type gate electrode on another region of the first wafer, and all of the gate electrodes are substantially parallel to one another.

8. (Original) The method of claim 7, wherein the first gate electrode includes a pFET, and the second gate electrode includes an nFET.

9. (Original) The method of claim 8, further comprising the step of applying at least one of a filled trench configuration and at least one film to provide:

a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET; and

a tensile stress applied in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET.

10. (Original) The method of claim 5, wherein each wafer includes a silicon layer on an insulator layer, and the opening forming step includes forming the opening to the silicon layer of the second wafer.

11. (Original) The method of claim 10, wherein the region forming step includes epitaxially growing silicon in the opening, and planarizing the silicon.

12. (Original) The method of claim 5, wherein the opening forming step includes forming a sidewall spacer along the opening.

13. (Original) The method of claim 5, wherein the first surface direction is a <100> surface

direction and the second surface direction is a <110> surface direction.

14. (Original) The method of claim 5, wherein the first surface direction is a <110> surface direction and the second surface direction is a <111> surface direction.

15. (Original) The method of claim 5, wherein the first wafer has a first surface orientation and the second wafer has a different second orientation, and the region has the second surface orientation.

16. (Original) The method of claim 5, wherein the first surface direction and the second surface direction are selected to degrade mobility.

17. (Currently Amended) A method of forming a semiconductor device structure, the method comprising the steps of:

bonding a first wafer having a first surface direction and a first surface orientation atop a second wafer having a different second surface direction and a different second surface orientation; the first wafer including a buried oxide layer;

forming an opening through the first wafer to a silicon layer of the second wafer;

generating a silicon in the opening to a surface of the first wafer, wherein the silicon has the different second surface orientation;

forming a plurality of pFETs on the silicon, and a plurality of nFETs on another region of the first wafer, wherein gate electrodes of the FETs are substantially parallel to one another; ~~and~~

applying at least one of a filled trench configuration and at least one process to provide:

a compressive stress in a longitudinal direction with respect to a current flow of the pFETs and a transverse direction with respect to a current flow of the nFETs; and

a tensile stress in a longitudinal direction with respect to a current flow of the nFETs and a transverse direction with respect to a current flow of the pFETs;

implanting oxygen; and

annealing to re-form the buried oxide layer prior to the FET forming step in the region that was removed when the opening was formed..

18. (Canceled).

19. (Original) The method of claim 17, wherein each wafer includes a silicon layer on an insulator layer, and the opening forming step includes forming the opening to the silicon layer of the second wafer.

20. (Original) The method of claim 17, wherein the region generating step includes epitaxially growing silicon in the opening, and planarizing the silicon, and the opening forming step further includes forming a sidewall spacer along the opening.

III. REMARKS

Claims 5, 7-17, and 19-20 are pending in this application. By this response, claims 5, 7 and 17 have been amended and claims 1-4, 6 and 18 have been canceled. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Furthermore, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 1-5 and 10-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Bryant et al. (U.S. Pat. Pub. No. 2005/0285187 A1), hereinafter "Bryant," in view of De Souza et. al (U.S. Pat. Pub. No. 2005/0116290 A1), hereinafter "De Souza." Claims 6-9 and 18 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Bryant and De Souza in view of Machesney et. al. (U.S. Pat. No. 5,670,388).

With respect to claims 5 and 17, Applicants submit that the cited references do not teach or disclose "implanting an oxygen; and annealing to re-form the buried oxide layer in the region that was removed when the opening was formed." In contrast to the claimed invention, Bryant, De Souza and Machesney do not teach removing a portion of a buried oxide layer, and then re-forming that layer after generating a silicon region with a different surface orientation. Although the references generally teach the forming of a buried oxide layer, they do not teach that such a layer is only re-formed in the regions where it was previously removed in order to form a region with a different surface direction as required by the claimed invention. See FIGS. 9-10 of the